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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Koos et al.

Attorney Docket No.:
NOVLP068/NVLS-000818

Patent: 7,338,908 B1

Issued: March 4, 2008

Title: Method for Fabrication of Semiconductor
Interconnect Structure with Reduced Capacitance,
Leakage Current, and Improved Breakdown Voltage

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on August 4, 2008 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____

Quyen N. Vuong

**REQUEST FOR CERTIFICATE OF CORRECTION
OF OFFICE MISTAKE
(35 U.S.C. §254, 37 CFR §1.322)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Certificate
AUG 11 2008
of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

CLAIMS:

1. In line 7 of claim 54 (column 16, line 28) change "copolymer" to -- coplanar --.
This appears correctly in the Amendment E as filed on August 28, 2007, on page 8, line 4.

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It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 504480 (Order No. NOVLP068/NVLS-000818).

Respectfully submitted,
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(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 7,338,908 B1

DATED : March 4, 2008

Page 1 of 1

INVENTOR(S) : Koos et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Claims:

In line 7 of claim 54 (column 16, line 28) change "copolymer" to --coplanar--.

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PATENT NO. 7,338,908 B1

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77. (new) A method of depositing a metal-containing capping layer on metal portions of a substrate containing a layer of metal and dielectric, the method comprising:

(a) receiving the substrate containing the layer of metal and dielectric;

(b) wet etching metal from the substrate from a position above or coplanar with an upper level of dielectric to a position below the upper level of exposed dielectric in the layer by contacting the substrate with a wet etching solution, wherein the etching solution oxidizes the metal of the substrate to a metal oxide, further comprising removing the metal oxide so that the exposed metal portions attain said position below the upper level of the exposed dielectric, wherein removing the metal oxide comprises contacting the substrate with an oxide etchant that selectively removes the metal oxide and not the metal, said oxide etchant comprising glycine;

and

(c) forming the capping layer on at least exposed metal portions of the substrate by electroless deposition.

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